Brent A. Thorne

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Portfolio: https://fractalclockwork.github.io/portfolio · GitHub: https://github.com/fractalclockwork · LinkedIn: https://linkedin.com/in/brent-thorne-a581554

Executive Profile

Research Engineer with over 20 years of experience in hardware–software co-design, high-performance computing (HPC), computational imaging, and real-time embedded systems. M.S. graduate from UC Berkeley's Molecular Science and Software Engineering (MSSE) program with expertise in CUDA optimization, parallel algorithms (MPI, OpenMP, UPC++), and reproducible simulation frameworks (GROMACS, LAMMPS, OpenMM). Proven track record in board bring-up, Linux kernel drivers, DMA data paths, scientific instrumentation, wireless stacks, and electro-mechanical system integration — including commercial firmware deployed at scale across consumer and utility endpoints.

Core Competencies

High-Performance Computing & AI: CUDA, MPI, OpenMP, UPC++, multi-GPU scaling; molecular dynamics (GROMACS, LAMMPS, OpenMM); PyTorch, TensorFlow, Computer Vision, SciPy, NumPy, Pandas, Jupyter.

Embedded Systems & Hardware: C, C++, Embedded Linux, kernel drivers, RTOS (ThreadX), bare-metal, Yocto, device trees; oscilloscopes, logic analyzers, JTAG; SPI, I2C, UART, CAN, Ethernet, USB, PCI-X, sub-GHz RF, LTE CAT-M, SDR.

Imaging, Signal Processing & Sensing: CT/radio reconstruction, cellular image analysis, automated artifact correction, fluorescence spectroscopy (RS-232/DAQ); V4L2, GStreamer, FFmpeg; FFTW, OpenCV, wavelet analysis; bioelectrical / EMG closed-loop sensing.

Mechatronics & Field Infrastructure: CNC, CAD/CAM, ECAD/PCB, FPGA (Verilog, Quartus), motor controllers, AC/DC power; remote observatories, telemetry, RF link budgets.

Representative Technical Projects

HPC Regression & Validation Framework (`hpc-runner`) | UC Berkeley
Architected an execution-agnostic benchmarking and automated regression engine (`hpc-runner`) supporting molecular dynamics workloads across heterogeneous cluster environments. Built containerized CUDA-enabled environments and validation scripts for parallel correctness, memory usage, and compute scalability.

Parallel Scientific Computing Optimization | UC Berkeley (CS267)
Implemented and benchmarked parallel algorithms using CUDA, MPI, OpenMP, and UPC++. Analyzed memory bandwidth saturation, thread divergence, and inter-node communication latency.

Hardware-in-the-Loop SDR & Real-Time Sensing Lab (`rad-lab` / `cede-labgrid`)
Designed containerized Software-Defined Radio and multi-MCU test environments for host-gated HWIL RF testing and protocol verification, with human assent gates, SIL→HWIL stages, and evidence reports.

Optical Spectrometer Control & Acquisition (`spectrometer-lab`)
Engineered Python RS-232 instrument control and acquisition software for a PerkinElmer LS 55 fluorescence spectrometer, implementing prompted DC1 protocol pacing, monochromator/slit positioning, serial-glitch taxonomy analysis, and Stage 1–3 verified emission scans.

FPGA Bring-Up Archive (`fpga-kit`)
Reproducible FPGA bring-up notes and toolchain continuity for Digilent Spartan boards on Xilinx toolchains — lab memory that keeps firmware work portable across tool churn.

Computational CT & Radio Imaging Reconstruction Pipeline | Freelance R&D
End-to-end CT and radio imaging workflows with custom reconstruction math and automated artifact correction; C++/CUDA acceleration of matrix transforms and signal processing loops converting raw multi-channel measurements into quantitative scientific visualizations.

Professional Experience

Research Engineer / Scientific & Systems Consultant

Freelance / Independent R&D · San Francisco, CA | Dec 2018 – Present

- Engineer integrated computational systems bridging physical instrumentation, embedded hardware, imaging modalities, and high-performance software.
- Develop GPU-accelerated C++/CUDA and Python pipelines for CT/radio image reconstruction, microwave resonant substrate analysis, and linear algebra modeling.
- Design ECAD schematics, PCB prototypes, and MCAD test fixtures to isolate hardware ambiguities and accelerate firmware validation.
- Architect automated CI/CD workflows, cross-compilation toolchains, and containerized deployment tools for heterogeneous compute targets.
- Conduct research in software-defined radio, high-rate sensor acquisition (V4L2, OpenCV), and active antenna array phase encoding.

Senior HW/SW Research & Development Engineer

GridNet · San Francisco, CA | Oct 2013 – Nov 2018

- Developed embedded radio modem firmware and Linux kernel networking drivers for sub-GHz smart-grid telemetry and LTE CAT-4/CAT-M M2M communication platforms.
- Architected SDR protocol analysis and signal processing tools to verify device interoperability and RF link reliability in high-interference industrial environments.
- Conducted cross-layer system debugging across custom RF hardware, firmware targets, and embedded Linux application runtimes.

Computer Scientist, Design Engineer & Inventor

Freelance Consultant · San Francisco, CA | May 2011 – Oct 2013

- Led mechatronic product development integrating CAD/CAM design, custom CNC programming, PCB layout, and embedded software.
- Designed bioelectrical signal acquisition front-ends and wavelet analysis pipelines for real-time physiological feedback systems.
- Managed multidisciplinary teams spanning electrical engineering, industrial design, and UI design.

Instructor / Educator & Community Mentor

TechShop & Humanmade · San Francisco, CA | 2012 – Present (Concurrent)

- Taught hands-on workshops in CNC machining, digital fabrication, microcontroller programming, CAD/CAM, and shop safety.
- Guided entrepreneurs and researchers through rapid prototyping, board bring-up, and mechanical assembly.

Operating Systems & Integration Engineer

OpenTV · San Francisco, CA & Amsterdam, NL | Oct 2004 – May 2011

- Developed embedded Linux device drivers, networking protocol stacks (TCP/IP, UDP, HTTP, PPP), and FAT/Ethernet subsystems for global digital television hardware.

- Managed global software releases and on-site driver integration across international hardware vendors, network operators, and broadcast providers.

Systems Engineer & Hardware Developer

Freelance / SFSU / EngineX / Net.World · San Francisco Bay Area | 1998 – 2004

- Engineered low-level C and ARM Assembly control path firmware for hardware-based TCP/IP TOE ASICs at Iready Corporation.
- Supported telescope computer control, image cataloging, and scientific computing systems as Observatory Operator & Computer Lab Consultant at San Francisco State University.
- Administered enterprise networking, CTI/VoIP routing, and thin-client infrastructure for Net.World and EngineX.

Education, Certifications & IP

Master of Science (M.S.) in Molecular Science and Software Engineering (MSSE)
University of California, Berkeley | 2026
Focus: High-Performance Computing, CUDA Parallel Programming, Molecular Simulation, AI/ML Software Engineering.

Certificate in Applied Data Science
Massachusetts Institute of Technology (MIT) | 2023
Focus: Deep Learning, Computer Vision, Machine Learning Workflows, Image Analysis.

Non-Matriculated Post-Baccalaureate Studies in Physics & Engineering
UC Berkeley & San Francisco State University | 2000 – 2022
Coursework: Mathematical Physics, Astrophysics, Classical Field Theory, Linear Systems Analysis, Control Systems, Power Electronics, Computational Linear Algebra, Bioinformatics.

Bachelor of Science (B.S.) in Electronics Engineering Technology
Hamilton Technical College | 1993

Patent: US Patent Application 61834836 — "System for Optimal Physical Exercise and Training" (Inventor). Closed-loop biometric monitoring and adaptive control integrating real-time bioelectrical signal processing, feature extraction, and physiological feedback.